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09/875,306	06/05/2001	Kazuhiko Terashima	450100-03272	7090

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,306	TERASHIMA ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 11/22/2005 has been entered. Claims 1-3 and 5-7 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 11/22/2005 have been fully considered but they are not persuasive. See explanation in the claim rejection below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al. U.S. 6,363,108 B1 in view of Fukasawa et al. U.S. Patent 5,920,591.

Regarding claim 1, as discussed in column 2 lines 3-20, inherent in the design of direct sequence spread spectrum communication systems is the requirement that a receiver must align its PN sequences to those of the base station, which distinguishes itself from other base stations by inserting a unique offset in the generation of its PN sequences. The PN sequence has a certain

length and corresponds to the claimed spread code. Agrawal et al. invention is related to a novel and improved method and apparatus for detecting a pilot signal at certain offset with a programmable matched filter searcher. Detecting a pilot signal at certain offset would be equivalent to detecting the timing of the spread code as appreciated by one of ordinary skill in the art. In view of that, the programmable matched filter searcher corresponds to the claimed synchronicity detection apparatus in the preamble.

Referring to figure 4, in column 11, line 54 via column 12 line 25, the programmable matched filter searcher comprising:

A PN generator is for generating PN sequences, which are used by a base station for spreading the signal to be transmitted. Hence, PN sequences are replica code of the spread codes.

Agrawal et al. does not expressly teach that the PN generator divides spread code advancing a phase of the spread code every certain period.

In column 6, lines 17-65, Agrawal et al. discloses an example of a search window size, L, of 64, and a coherent accumulation of 256 is desired. The initial tap values, corresponding to a PN sequence, appropriate for the beginning of the window are loaded into despreader 420, see column 6, lines 20-31. After the window size of 64 cycles, a new set of taps values for despreader 410 has been calculated and the matched filter procedure is repeated again for another 64 cycles. The process is repeated twice more, *changing the taps each time* until the accumulators have accumulated four 64 chips values for the desired C of

256. Also disclosed in column 6 line 65 through column 7 line 32, Agrawal et al. expresses that the loading of PN tap values is performed as follows: the PN sequences will be generated differently depending on whether the same set of hypotheses is to be tested or a new set is beginning. In the case of 64 cycles as recited above, the PN generators have moved forward 64 chips. In view of that, it would have been obvious for one of ordinary skill in the art at the time the invention was made that by loading a new set of tap values for every 64 cycles, the PN generator as taught by Agrawal et al. equivalently divides the spread code advancing a phase of the spread code *every certain first period*, e.g. in this case, a certain period is 64 cycles, to generate a set of taps of a PN sequence, which corresponds to a replica code of the spread code. The motivation is that the act of moving forward 64 chips four times for C=256 would be equivalent to dividing the claimed spread code into four 64 chips.

Referring back to figure 4, also in column 11 line 54 through column 12 line 20, the matched filter, in the form of despreader 410, summers 420 and 422 for I and Q values, I coherent accumulator 430, Q coherent accumulator 432, energy calculator 440, for performing despreading I and Q channel data with PN sequences. The act of despreading is equivalent to the detection of correlation values of the PN sequences. In the example recited above, the matched filter size is equal to the window size of 64 chips. Hence, the matched filter performs correlation between the PN sequence and reception signal every 64 cycles. Furthermore, in column 4 lines 60-67, referring to figure 4 of Agrawal et al.

invention, Agrawal et al. teaches that each matched filter structure comprises an N-value shift register for receiving data. In column 7 lines 1-15, Agrawal et al. further teaches that the matched filter is N values wide so an N bit tap sequence must be generated. In light of the foregoing discussion, the act of despreading is performed every period, corresponding to the claimed every certain second period.

Agrawal et al. does not teach a pseudo-random sequence generation means which generates a pseudo-random sequence from an initial value after supplying said pseudo-random sequence generated as said replica code as claimed in the application claim.

Referring to figure 1, Fukasawa et al. discloses a spreading code generator 2 utilizing a linear-feedback shift register based PN generator 14. In column 3 line 5 via column 4 line 35, the spreading code generator 2 comprises two spreading code generating circuits 4 and 6 and modulo-two adder 8. The first spreading code generating circuit 4 receives a framing signal FS, a chip clock signal CK, and initialization data Si, and generates a first spreading code Sp at intervals determined by the framing signal FS. The second spreading code generating circuit 6 receives the chip clock signal CK and framing signal FS and a control parameter Sc to generate a second spreading code So. The modulo-two adder 8 produces a third spreading code Ss. Figure 2 shows waveforms of the framing signal FS, chip clock signal CK, reset signal Sr, and first spreading code Sp. The PN generator 14 in figure 2 is reset to the same initial state at

every reset signal Sr. The chip sequence of the first spreading code Sp repeats at intervals. In light of the foregoing discussion, the third spreading code Ss corresponds to the claimed replica code and pseudo-random sequence; the initialization data Si corresponds to the claimed initial value; and spreading code generator 2 corresponds to the claimed pseudo-random sequence generation means.

Agrawal et al. and Fukasawa et al. teachings are similar in that both inventions uses linear-feedback shift register (LFSR) PN generators for generating PN sequences as replica codes. Fukasawa et al. invention differs from Agrawal et al. invention in that Fukasawa et al. does not show the spreading code generator generating I and Q PN sequences. Nevertheless, Fukasawa et al. spread code generator can be modified to produce I and Q PN sequences as appreciated by one of ordinary skill in the art. Fukasawa et al. teachings show LFSR based spread code generators designed for both transmitting and receiving at all stations. Hence, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Agrawal et al. invention can be modified to utilize the spread code generator, as taught by Fukasawa et al.. The motivation is that PN generator is well known in the art. The advantages of Fukasawa et al. are that the spreading code generator can be used for both transmitting and receiving at all stations. Another further advantage is the spreading code generator enables each mobile station to have a unique pseudorandom synchronization signal.

Regarding to newly added limitations, in column 4 lines 60-67, referring to figure 4 of Agrawal et al. invention, Agrawal et al. teaches that each matched filter structure comprises an N-value shift register for receiving data. In column 7 lines 1-15, Agrawal et al. further teaches that the matched filter is N values wide so an N bit tap sequence must be generated. Therefore, in view of the foregoing disclosure, every certain first period is the time interval generated by the N shift time.

Regarding claim 2, figure 4 further shows a non-coherent accumulator 450, which is disclosed to be similar to accumulators 430 and 432, see column 7 lines 45-60. The coherent accumulators 430 and 432 are RAM based. During each cycle, the appropriate partial accumulation is retrieved, added to the output of either summer 420 or 422, and the resultant partial accumulation is stored in the RAM again; see column 6 lines 30-42. In view of the foregoing disclosure, the non-coherent accumulator 450 has a memory (e.g. RAM memory), which accumulates the result of each offset in the form of output energy from the energy calculator 440. Output energy is representative of the correlation values detected by the matched filter every 64 cycles, corresponding to the claimed certain first period. Because the non-coherent accumulator 450 performs similar functions as coherent accumulators 430 and 432, non-coherent accumulator 450 retrieves partial accumulation stored in the RAM and adds it to the output of the energy calculator 440. Equivalently, the non-coherent accumulator 450 cyclically adds the

correlation values detected by the matched filter in the form of energy as claimed in the instant application.

In column 7 lines 60-67, the results of non-coherent accumulator 450 are delivered to DSP 460 where the values are examined to determine which offset in the search window likely corresponds to the location of a pilot signal. In view of the foregoing, DSP 460 corresponds to the claimed means for detecting correlation energy from non-coherent accumulator 450.

Regarding claim 3, referring to figure 4, the combination of sum 420 coherent accumulate 430 for the I component, and sum 420 coherent accumulate 430 for the Q component, each constitutes to the claimed adding means for the following reasons:

- in column 6 lines 15-65, in the example of matched filter size, N = 64, search window size, L, = 64 and a coherent accumulation, C = 256, the results of each cycle, outputted from the summers 420 and 422, are loaded into coherent accumulators 430 and 432, respectively. The accumulators 430 and 432 are RAM based. During every 64 cycles, the appropriate partial accumulation is retrieved, added to the output of either summer 420 or 422, and the resultant partial accumulation is stored again in the RAM. In view of the foregoing discussion, the accumulators 430 and 432, holding appropriate partial accumulations, effectively delay outputs of the matched filter for I and Q components every 64 cycles, which corresponds to the claimed certain first period as

discussed in claim 1. The act of holding partial accumulation is equivalent to delaying the output of the matched filter. Agrawal et al. does not show the combination of sum and coherent accumulate generates a delayed signal, adds the delayed signal and the output of the matched filter. However, as recited above, the partial accumulation is retrieved and added to the output of either summer 420 or 422. In view of that, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the act of retrieving partial accumulation and added to the output of either summer 420 or 422 is equivalent to the claimed generating a delayed signal and added to the output of the matched filter. The motivation is retrieving partial accumulation is equated to the step of generating a delayed signal, and adding to the output of either summer 420 or 422 is equated to adding the partial accumulation and output of the matched filter for each component I or Q.

- Figure 4 further shows a DSP 460 for detecting the correlation energy from output of the non-coherent accumulator 450.

Regarding claim 5, the PN generators as taught by Agrawal et al. correspond to the claimed correlation coefficient generation means.

The PN sequences are generated via linear-feedback shift register based PN generators. In view of that, the linear-feedback shift register corresponds to the claimed register for generating a certain pseudo-random sequence, see column 7, lines 1-32.

In column 7, lines 1-31, after every 64 chip cycles, the PN generators moved forward 64 chips. Hence, the act of moving forward N chips, corresponding to the claimed operation means, phase shifts a phase of the pseudo-random sequence generated by the linear-feedback shift register as discussed above.

The PN generators load or output the tap values into despreader 410 for every 64 chip cycles for a N-chip coherent accumulation. Hence, the PN generators provide a mean for supplying phase shifted pseudo-random sequence every 64-chip cycles, which correspond to the claimed means for supplying as set forth in the claim.

Regarding claim 6, referring back to the example in column 6 lines 17-65 of Agrawal et al. invention, for a coherent accumulation, C = 256, the matched filter size, N = 64, and window size, L = 64, in the following rejection, 64-chip cycles corresponding to the matched filter size is equated to the claimed one unit of the spread code. The N-chip coherent accumulation is equated to the claimed spread code. Furthermore, the claimed one unit of first inputted spread code, the claimed one unit of second spread code, and the claimed one unit of next spread code *are assumed to be replica codes in the same spread code cycle in light of the original disclosure* (see page 11 line 1 through page 12 line 12; page 14, lines 14-27).

In column 6 lines 17-65 of Agrawal et al. invention, after the first 64 cycles passed, a new set of taps for the despreader 410 have been calculated and loaded into despreader 410. These are calculated so that the same 64 offset hypotheses that were tested in the first pass can be tested again. In view of the foregoing discussion, the new set of taps for the next 64-chip cycles is calculated from the first 64-chip cycles. As recited above, the 64-chip cycles is equated to the claimed one unit of the spread code cycle. The pseudo sequence corresponding to the 64-chip cycles is equated to the claimed replica code as claimed in claim 1. The process is repeated two more, changing the taps each time until the accumulators have accumulated four 64-chip values for the desired C of 256. Each new set of taps is calculated from previous 64-chip cycles.

Agrawal et al. does not expressly show a spread code generation means as set forth in the application claim. However, Agrawal et al. PN generators perform similar function as the spread code generation means. Even though Agrawal et al. does not show a spread code generation means as set forth in the application claim, a person of ordinary skill in the art would have recognized the interchangeability of the PN generators shown in Agrawal et al. invention and the correlation coefficient generation means disclosed in the claim. As result of a prima facie case of equivalence, the PN generators would include a spread code generation means for performing similar function as the claimed spread code generation means as set forth in the claim.

Regarding claim 7, Agrawal et al. teaches the PN generators are linear feedback shift register based PN generators. In the example of window size

equal to 64, and the matched filter size of 64, the PN generators generate pseudorandom sequence of 64 chip cycles, which corresponds to the claimed one unit of the spread code.

Agrawal et al. does not show one unit of the spread code is generated by repeating latch operations as set forth in the application claim.

Referring to figure 1, Fukasawa et al. discloses a spreading code generator 2 utilizing a linear-feedback shift register based PN generator 14. In figure 3, in column 4, lines 24-60, the PN generator 14 comprises latches 26 and modulo-two adders 28. At every cycle of chip clock signal CK, the value in each latch 26 is shifted into the next latch to the right with feedback through the modulo-two adders 28 to the leftmost latch. The PN generator 14 outputs one chip of the first spreading code Sp. Referring to figure 1, the modulo-two adder 8 adds modulo two the chip-wise sum of the first and second spreading codes Sp and So to produce a third spread code, see column 3, lines 27-35.

Agrawal et al. and Fukasawa et al. teachings are similar in that both inventions uses linear-feedback shift register (LFSR) PN generators for generating replica codes. Agrawal et al. invention differs from Fukasawa et al. invention in that Agrawal et al. does not show the latch operations for generating spreading code. Fukasawa et al. does not show the spreading code generator generating I and Q PN sequences. Nevertheless, Fukasawa et al. spread code generator can be modified to produce I and Q PN sequences as appreciated by one of ordinary skill in the art. Fukasawa et al. teachings show LFSR based

spread code generators utilizes latch operations to generate chip codes, and is designed for both transmitting and receiving at all stations. Hence, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Agrawal et al. invention can be modified to utilize the spread code generator, as taught by Fukasawa et al.. The motivation is that PN generator is well known in the art. The advantages of Fukasawa et al. are that the spreading code generator can be used for both transmitting and receiving at all stations. Another further advantage is the spreading code generator enables each mobile station to have a unique pseudorandom synchronization signal.

In column 4, lines 40-55, in figure 3, Fukasawa et al. discloses the value in each latch 26 is shifted into the next latch to the right at every cycle of chip clock signal CK. The value in the rightmost latch is output as one chip of the first spreading code Sp. Hence, for a window size equal to 64, and a matched filter size of 64 in Agrawal et al. invention, Fukasawa et al. spreading code generator latch 64 times for a 64 chip sequence. In view of that, Agrawal et al. and Fukasawa et al. teachings address the claimed limitations.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 02/15/2006

Examiner KHANH TRAN